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A 1280x960 2.8µm HDR CIS with DCG and Split-Pixel Combined

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A triple capture high dynamic range (HDR) CMOS image sensor with an active array size of 1280x960, and 0.8e- rms noise floor is presented. This is the first sensor that combines split-diode pixel technology [1][3] with dual conversion gain (DCG) readout [2] to achieve HDR with LED flicker mitigation (LFM). The pixel size is 2.8um, which is the smallest split-diode pixel reported to date, implemented in OmniVision's 2nd generation BSI process (BSI2) with buried deep trench isolation (BDTI) for low crosstalk (fig. 3). The sensor delivers three capture values: two from the large photo diode (LPD) exposure sensed at both high conversion gain (HCG) and low conversion gain (LCG), and one from the small photodiode (SPD) exposure sensed at LCG. The three captures (HCG, LCG, and SPD) are read out using digital correlated double-sampling (DCDS) with 10b ramp ADCs and then combined digitally to form a 20b linear output pixel value.

A pixel circuit diagram and readout timing diagram is illustrated in Fig. 1 and 2, respectively. The floating diffusion nodes for LPD (FD1) and SPD (FD2) are separated by the DFD transistor. Low CG is obtained by asserting DFD to increase the total equivalent capacitance at the gate of the pixel source follower transistor (SF). High CG is obtained by de-asserting DFD. The LPD charge can be sensed at both LCG and HCG, whereas SPD can only be read out in LCG mode.

Fig. 3 illustrates a zoom-in of 4x4 pixels with Bayer color filter array (CFA) pattern. SPD and LPD are positioned diagonally to each other in order to maximize fill factor and optical performance.

The sensitivity ratio between the LPD and the SPD is approximately 100:1 (see figs. 7 and 8 for details). Reduced sensitivity on SPD is needed for LFM to function correctly, because it enables use of longer exposure times without saturating the photodiode. Thanks to a TiN-based neutral filter placed in the optical stack between the photodiode and the color filter, it is possible to desensitize SPD and to tune its sensitivity by adjusting the material thickness. A cartoon illustration of the above mentioned process features is provided in fig. 4.

Exposure time is controlled independently for LPD and SPD in order to obtain the desired overall responsivity ratio and dynamic range (fig. 5). The split-diode architecture enables overlapping exposure for LPD and SPD. This is beneficial to reduce artefacts arising from motion or from light source flicker in the scene [3]. Another benefit is that the readout of the exposure values is aligned, removing the need for additional line-buffers to combine the values; thus minimizing die size and power dissipation.

Fig. 6 shows the chip architecture. In order to output HDR processed images at 30fps, the A/D conversion rate needs to be equivalent to 90fps. Column-parallel single-slope A/D converters were implemented to conserve power dissipation. The correlated double sampling was implemented in the digital domain (DCDS) to suppress ADC offsets, and to minimize vertical FPN (VFPN). The black level correction (BLC) has individual correction for the exposure channels. Separate lens correction (LENC), and color correction matrix (CCM) is applied to the SPD channel to align with the LPD response. If the LFM processing block detects flicker on the LPD pixel values, the LPD value will be replaced by SPD (linearized), because SPD has constrained integration time to >11ms. Before data is output on MIPI or DVP, the pixel values can be piecewise linearly (PWL) mapped from 20-bits to 12-bits.

Quantum efficiency (QE) was measured for both LPD and SPD (fig. 7 and 8). A peak QE of 70% at 530nm was measured for LPD. Fig. 8 shows the QE curve for SPD, which is typically 100x lower than LPD (wavelength dependent). Higher color crosstalk

in SPD is compensated by dedicated LENC and CCM in the SPD data path.

Results from blooming tests are provided in fig. 9. No LPD-to-SPD blooming is observed since the SPD response remains linear (straight line) with increased saturation on neighboring LPD (when light level increases).

The 3.3V AVDD pixel supply is regulated on-chip. The power supply rejection ratio (PSRR) has been measured on LPD at high CG, which is most critical for low-light performance (fig. 10). At both 8x and 15.5x analog gain, the maximum PSRR value is approximately -32dB at around 2MHz. This means that the sensor can deliver excellent noise performance even in applications with noisy power supply.

A scene with a pulsed LED source was used to compare performance with and without the LFM algorithm activated. Neutral white (4300K) LEDs are biased to approximately 9.5lm during active period. Pulse frequency is 100Hz and duty cycle is set to 10% (1 ms pulse width). Distance from LED source to camera is about 0.4m. LPD exposure time is 4.1ms, and SPD is set to10ms. The sensor is running in 20b combined mode with output values PWL compressed to 12b.

Captured images are shown in figs. 11, 12, and 13 with the LED-vs-sensor exposure timing illustrated at the top right corner. These captures demonstrate how LED flicker is mitigated when the LFM function is enabled. Also illustrated is the fundamental limitation of intensity modulation in the output images due to varying degree of exposure overlap. The industry is still looking for cost- and power-efficient solutions to address this complex problem.

An overview of the sensor performance parameters is provided in Table 1.

References:

[1] T. Willassen et al., “A 1280x1080 4.2µm Split-diode Pixel HDR Sensor in 110 nm BSI CMOS Process”, IISW 2015

[2] J. Solhusvik et al., “A 1392x976 2.8µm 120dB CIS with Per-Pixel Controlled Conversion Gain”, IISW 2017

[3] J. Solhusvik et al., “A comparison of high dynamic range CIS technologies for automotive applications”, IISW 2013

[4] C. Silsby et al., “A 1.2MP 1/3” CMOS Image Sensor with Light Flicker Mitigation”, IISW 2015

[5] S. Iida et al., “A 0.68e-rms Random-Noise 121dB Dynamic-Range Sub-pixel architecture CMOS Image Sensor with LED Flicker Mitigation”, IEDM, Dec. 2018

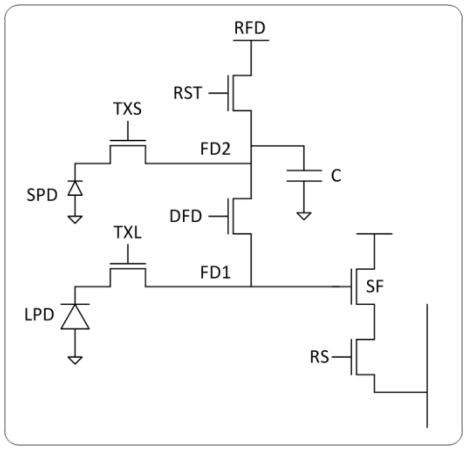


Figure 1

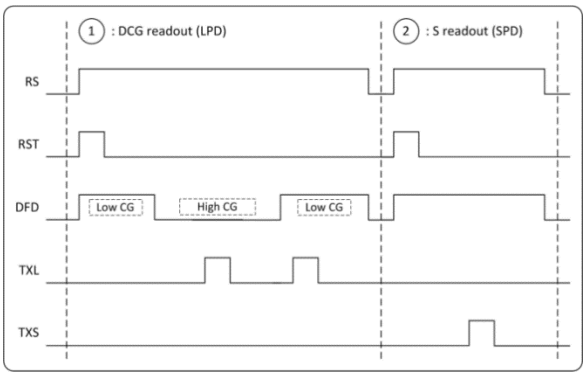
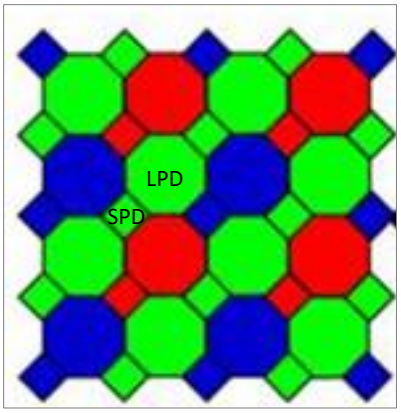


Figure 2



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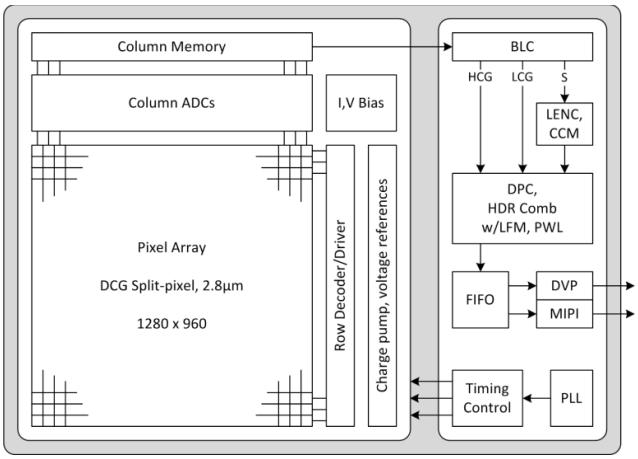


Figure 6

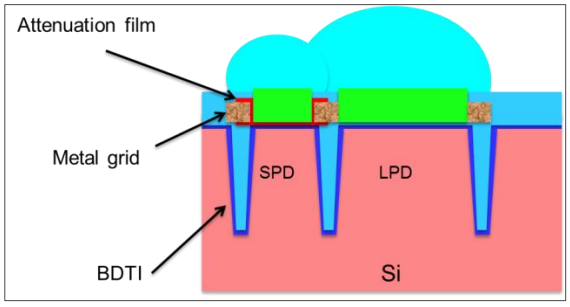


Figure 4

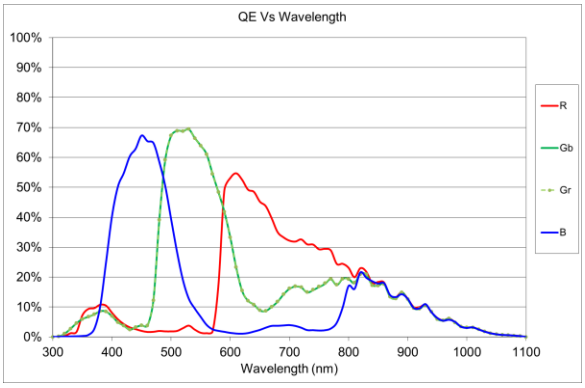


Figure 7

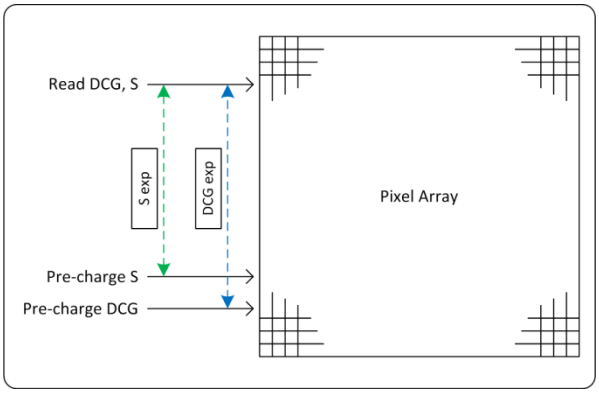
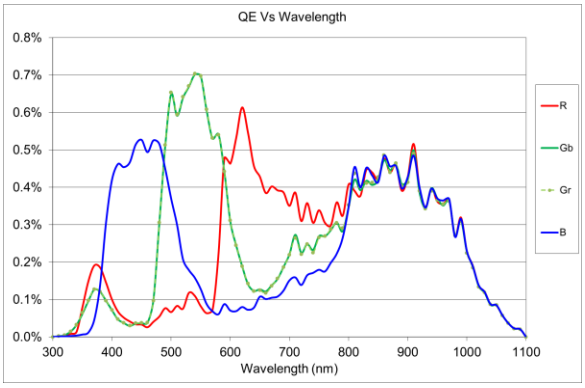


Figure 5



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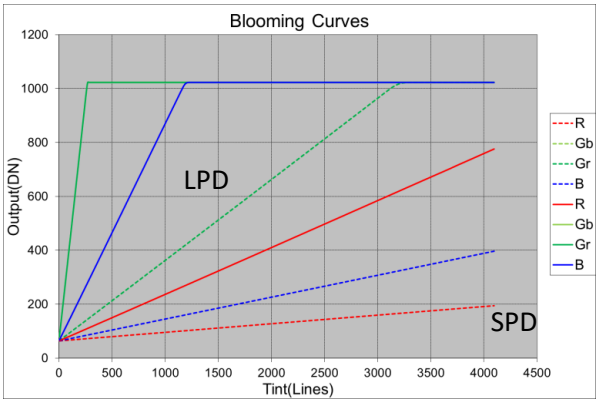
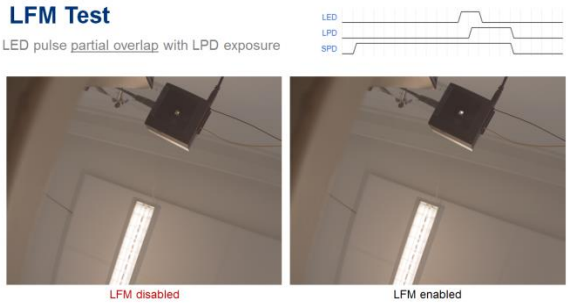


Figure 9



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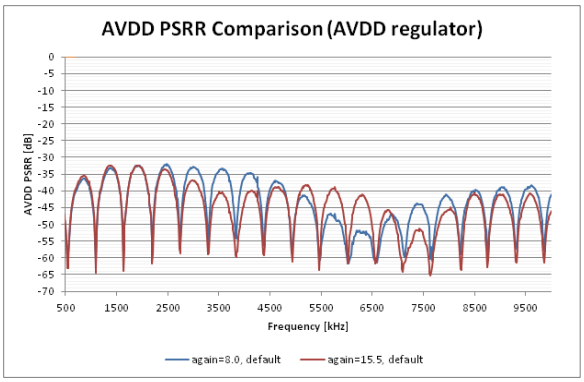

Figure 10

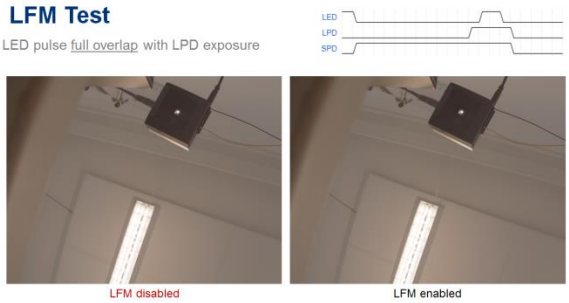

Figure 13

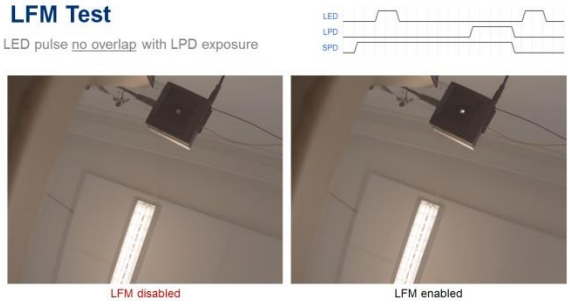

Figure 11

Optical Format	1/4”	
Pixel Size	2.8 µm	
Effective pixels	1288 x 968	Incl. border
Maximum frame rate	30 fps	@HDR, full res
ADC resolution	10 bits	
Responsivity (530nm)	24600 e-/Lux.s	LPD
	238 e-/Lux.s	SPD
Temporal read noise@RT and 16x gain	0.83 e-rms	LPD, HCG
	3.05 e-rms	LPD, LCG
	2.96 e-rms	SPD, LCG
Total FPN @25C, and 16x gain	0.21 e- rms	LPD, HCG
	0.80 e- rms	LPD, LCG
	0.34 e- rms	SPD, LCG
Conversion gain	200uV/e-	HCG
	49uV/e-	LCG
Dark current @60C	4.2e-/s	SPD
	25.6e-/s	LPD
Lag (high-light/low-light)	0.39e- / 0.7e-	SPD
	0.3e- / 1.1e-	LPD LCG
	0.05e- / 0e-	LPD HCG
Full-well-capacity	7900e-	SPD
	22000e-	LPD
Power (analog/digital/IO)	79/72/34mW	25C, 30fps, MIPI

Table 1